Proposed Claim Amendments

1. (Twice Amended) A memory array, comprising:

a common write word line shared by a first memory bank and a second memory bank;

a first write buffer having [an] a first input to receive a first control signal, a second input to receive a data signal, and two or more outputs for asserting an encoded output signal, the first write buffer [capable of] encodes the data signal and drives [driving] a first bit line and a second bit line of the first memory bank with [an] the encoded [output] signal in response to [selected by] the first control signal, the first write buffer driving each of the outputs when the first control signal is in a selected state so a selected cell of the first memory bank holding a data value maintains the data value when the first control signal is in the selected state; and

a second write buffer having [an] a first input to receive a second control signal, a second input to receive a data signal, and two or more outputs for asserting an encoded output signal, the second write buffer [capable of] encodes the data signal and drives [driving] a first bit line and a second bit line of the second memory bank with [an] the encoded [output] signal in response to [selected by] the second control signal, the second write buffer driving each of the outputs when the second control signal is in a selected state so a selected cell of the second memory bank holding a data value maintains the data value when the second control signal is in the selected state;

8. (Twice Amended) A memory array comprising:

a plurality of memory banks for storing data;

a common write word line shared by the memory banks;

a plurality of write buffers wherein each write buffer is associated with one of the memory banks; and

a writing module within each of the plurality of write buffers for driving a plurality of bit lines in each of the associated memory banks with [an] a plurality of encoded output signals, at least one of the encoded output signals encoded in a manner to prevent an overwrite of stored data in at least one of the memory banks.

14. (Amended) In a banked memory array having a common word line shared by the banks of the memory array and write buffers for each of the memory banks, a method for writing data into the banked memory array, said method comprising the steps of:

initializing the memory array to write data into the memory array by activating the write word line;

providing each of the write buffers with data;

selecting one of the write buffers to write data into a selected one of the memory banks;

encoding the data in each of the write buffers before the selected write buffer writes the data into the selected one of the memory banks, wherein the encoded data in the selected write buffer is in a first state and the encoded data in the other write buffers is in a second state; and

driving the encoded data into each of the memory banks, wherein the data encoded in the first state over writes data held by the selected memory bank and the data encoded in the second state prevents data held by the other memory banks from being overwritten.

18. (Amended) A memory array comprising:

a common write word line;

a plurality of memory banks for storing data,

a plurality of write buffers each having an input to receive a control signal, wherein each of the write buffers [are] is associated with one of the memory banks; and

logic within the write buffers for [sending] driving a different set of encoded signals to at least two of the memory banks in response to the control signal, wherein one set of encoded signals driven by the logic within the write buffers indicates a data write in a first of the at least two memory banks and a second set of encoded signals driven by the logic within the write buffers indicates a memory cell in a second of the at least two memory banks should maintain state.